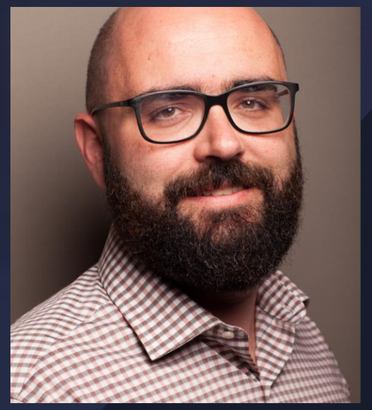
FPGAs e SoCs
De monstros à solução no edge

João Dullius
BP&M

O palestrante



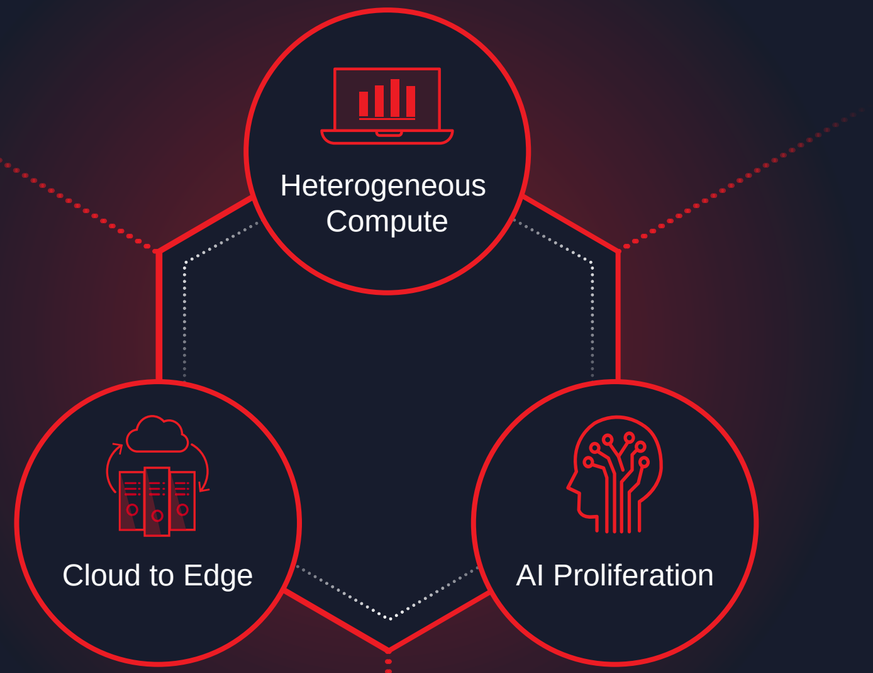
João Dullius
BP&M Representações
joaodullius@bpmrep.com.br

- Engenheiro de Aplicações
  - Processamento Embedded
  - FPGAs

BROADCOM
AVAGO TECHNOLOGIES Authorized Representative
XILINX
Littelfuse
Micron
FINISAR
IDT
Pulse Electronics
Insight SiP It's all in the package
TELINK SEMICONDUCTOR
GaN Systems
EVE ENERGY VERY ENDURE
ZETTLER AMERICAN ZETTLER.INC.
Grayhill Intuitive Human Interface Solutions
NORTHFORGE

- Industry Trends
- The Monster
- The Solution
- What about Rhinos?

Industry Trends



Internet of Everything

VoT - Video of Things

VoT - Video of Things

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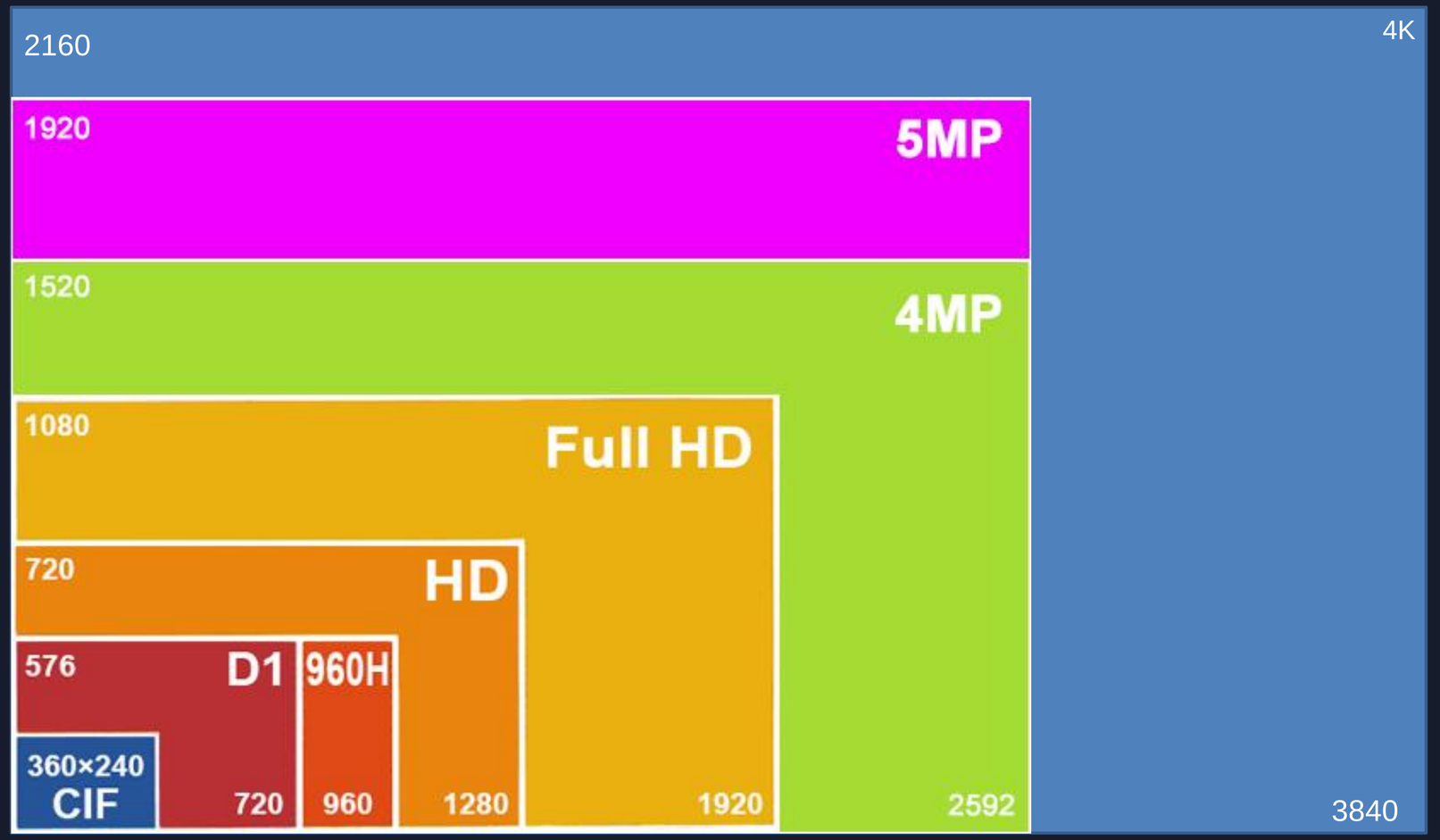
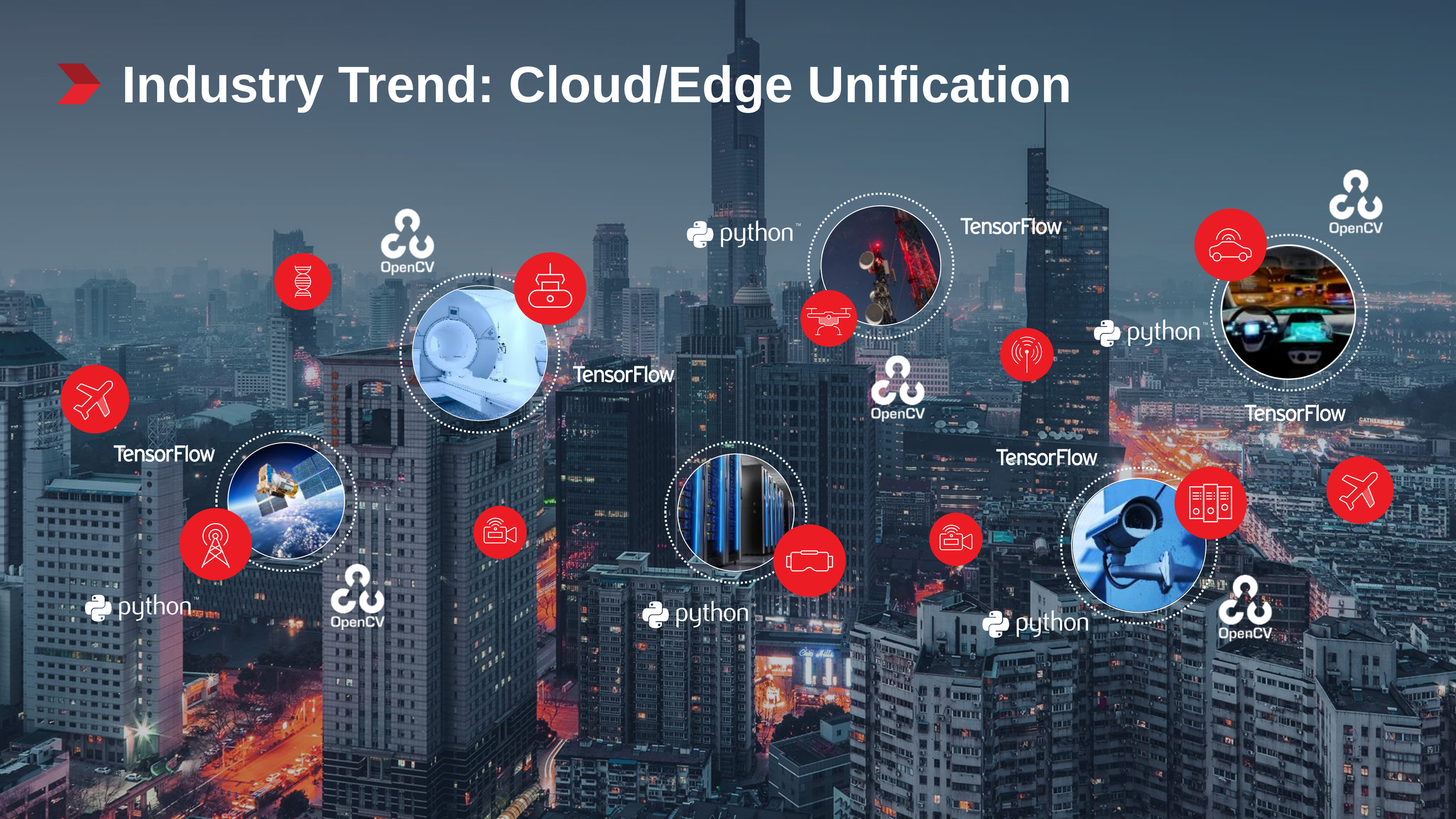
VoT - Video of Things



VoT - Video of Things

Resolution	H.264	MJPEG
1MP (1280*720)	2 Mbps per camera	6 Mbps per camera
2MP (1920*1080)	4 Mbps per camera	12 Mbps per camera
5MP (2560*1960)	10 Mbps per camera	30 Mbps per camera
4K (3840*2160)	18 Mbps per camera	64 Mbps per camera

Industry Trend: Cloud/Edge Unification



Industry Trend: AI Proliferation

Power efficient inference along with traditional software

Data Center

5G

Autonomous Driving

Security

Genomics

Video Analytics

Healthcare

Finance

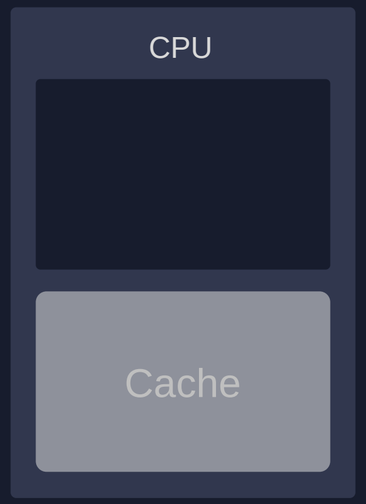
Industry Trend: Heterogeneous Compute

SINGLE CORE

1980-2000

2x/ 1.5y

process → Dennard scaling

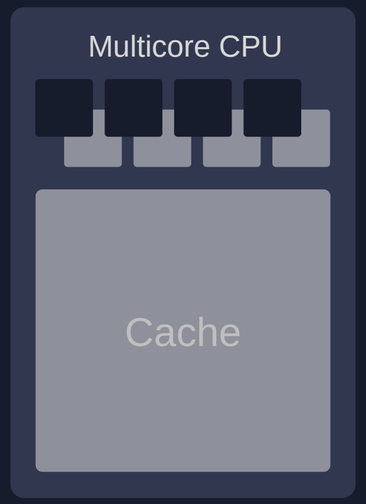


MULTICORE

2000-2010

2x/ 3.5y

multithreading → Amdahl's law

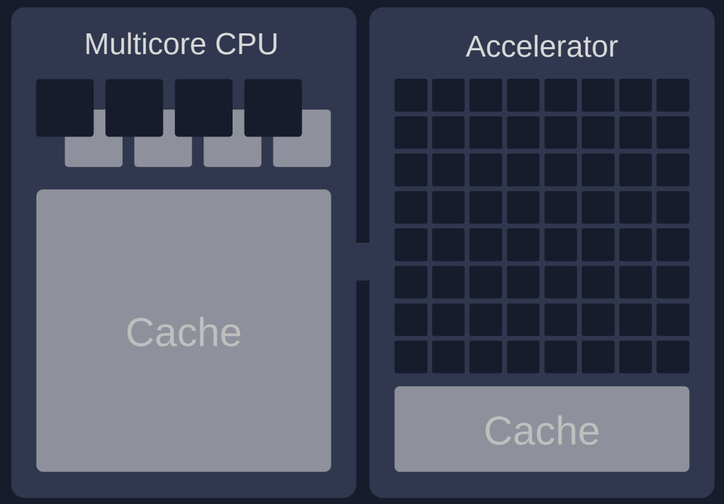


HETEROGENEOUS

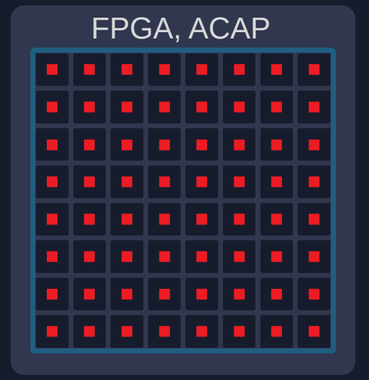
2010-2020

2x/ 10y

density → Moore's law

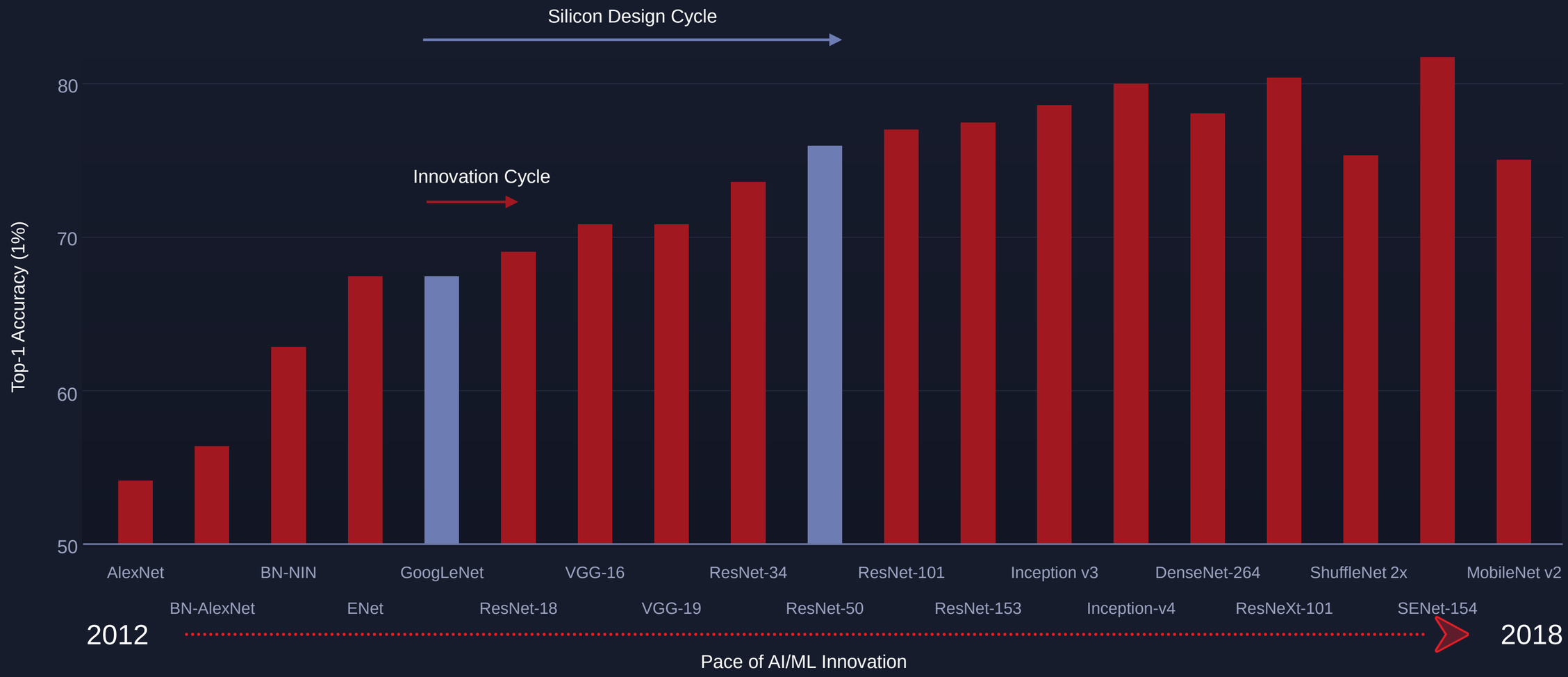


ADAPTIVE HETEROGENEOUS

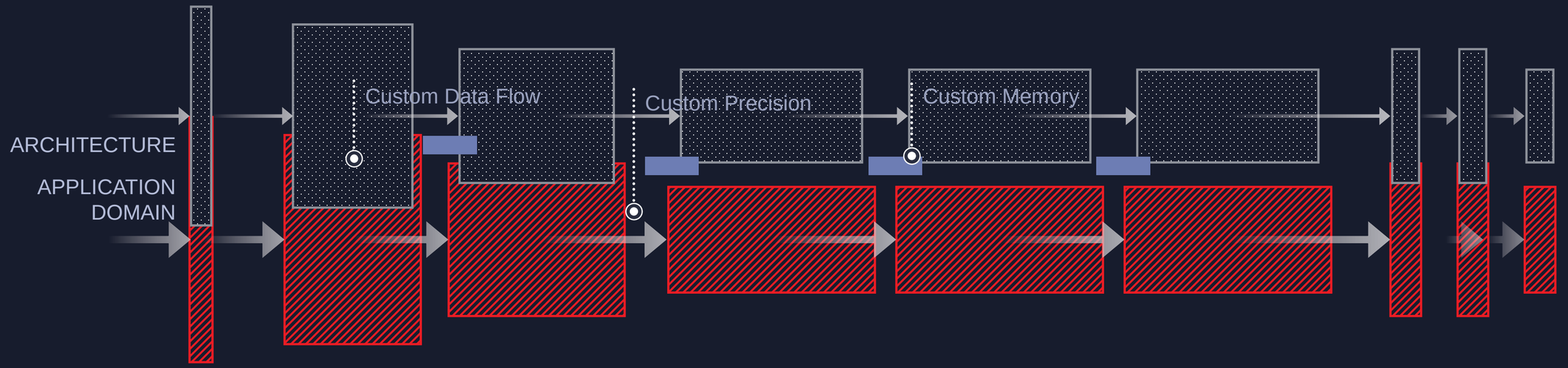


Scaling from: Silicon process → Architecture-aware software → Software-aware architecture

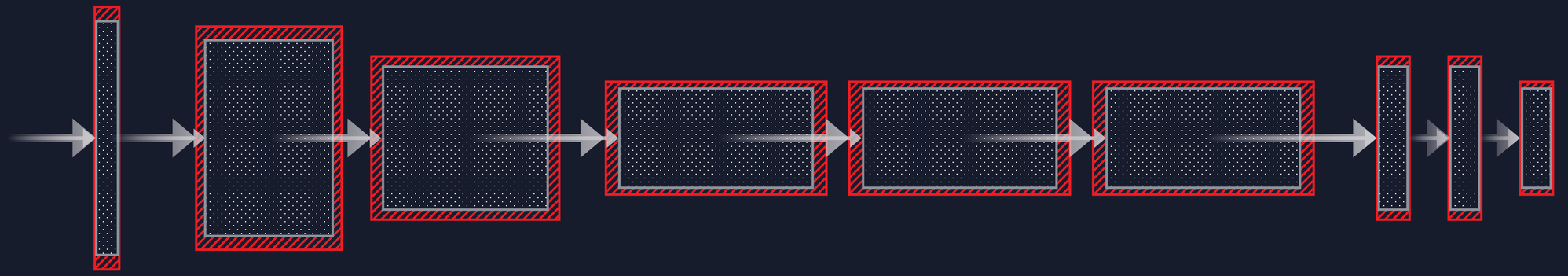
Speed of Innovation Outpaces Silicon Cycles



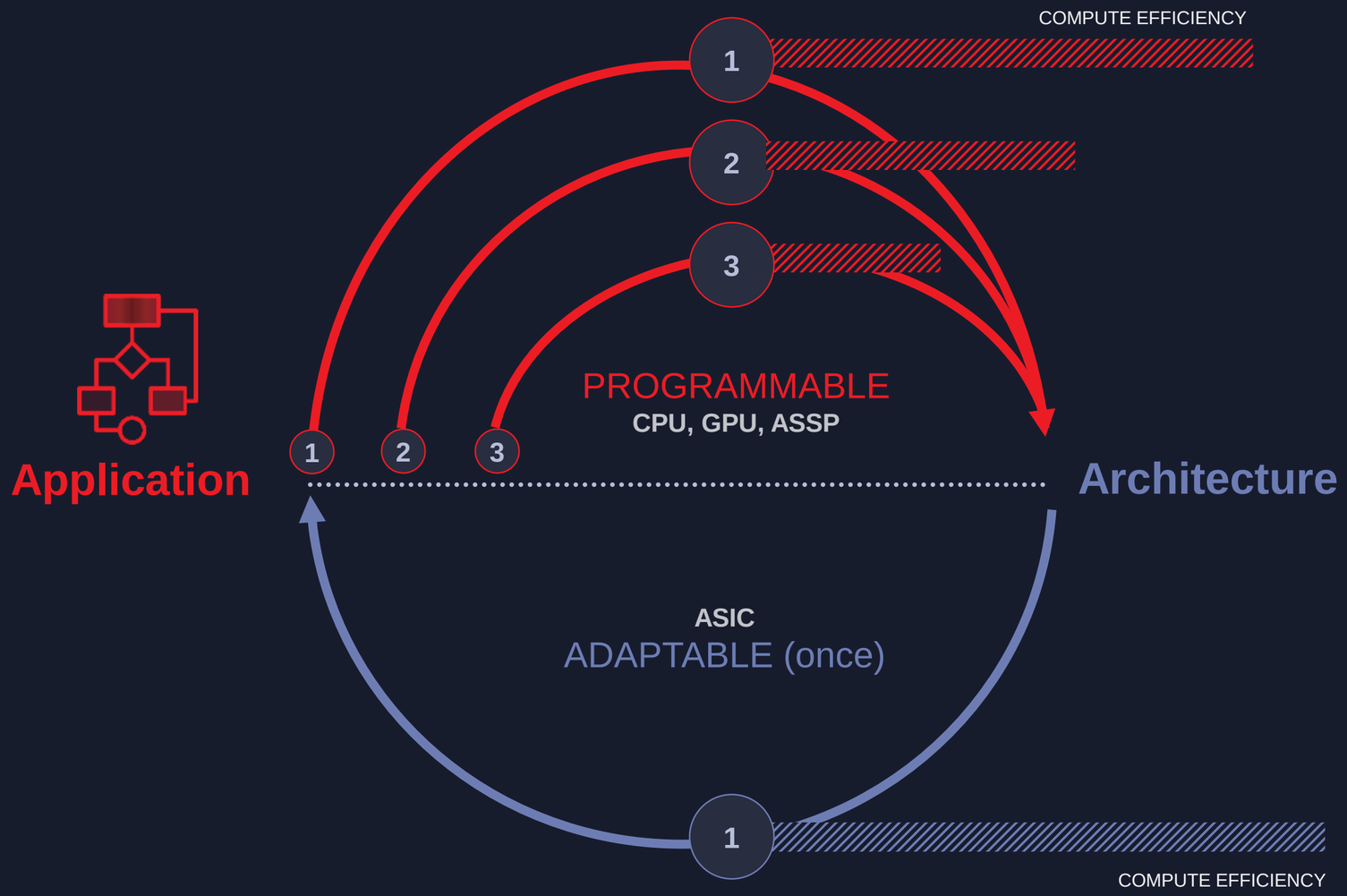
Architecture Adaptability



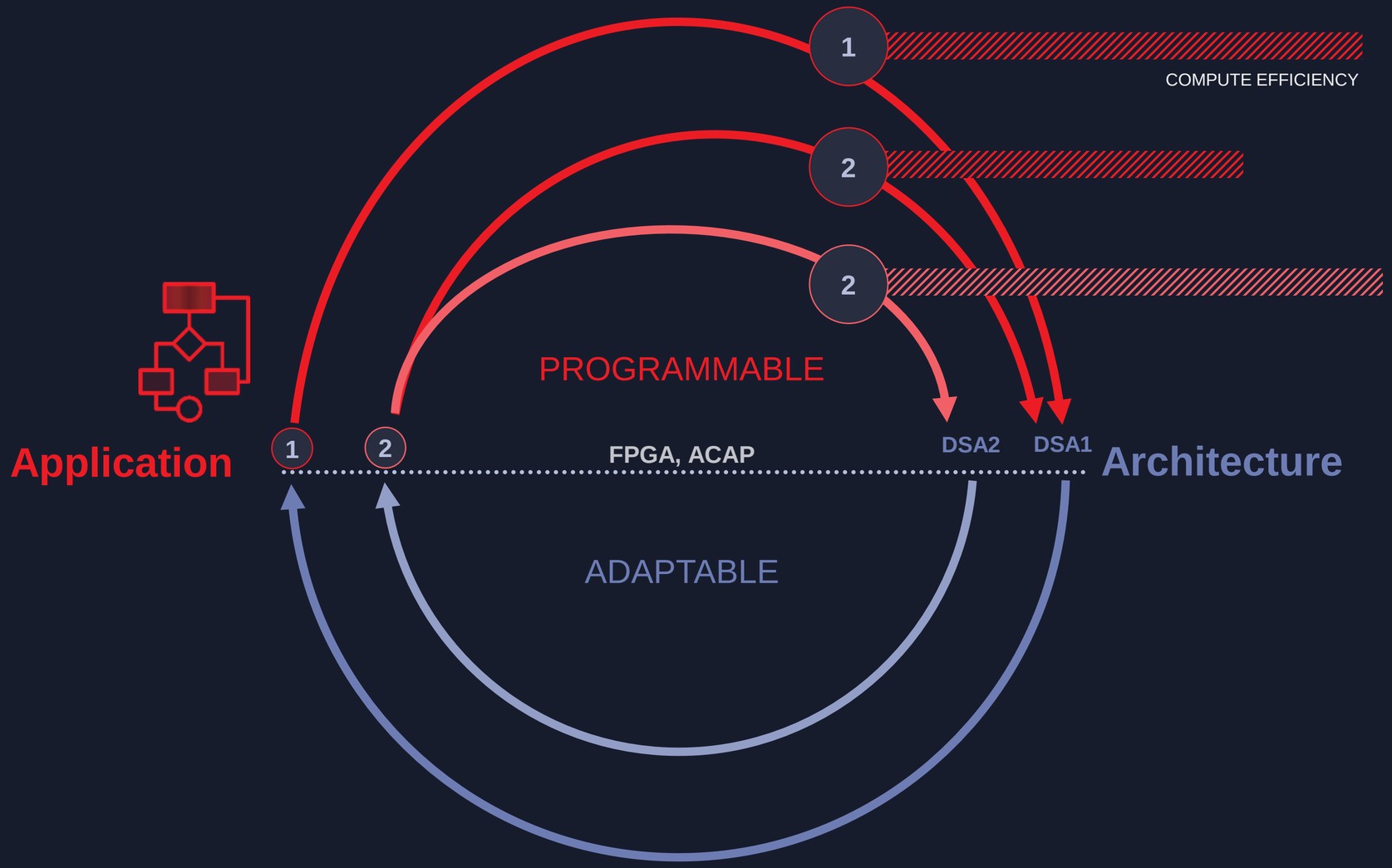
ARCHITECTURE ADAPTABILITY



Programmable OR Adaptable



Why Not Programmable AND Adaptable?



Deep Learning vs. Traditional Software

Deep Blue (traditional software)
beats Garry Kasparov

Complexity: 10^120

IBM Watson becomes
Jeopardy champion!

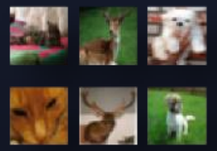


Image
classification

Classification
better than humans

AlphaGo beats
Lee Sedol

AlphaZero
chess champion!

ADAS

Robo-taxis
(geofenced)

Fully
autonomous
vehicles

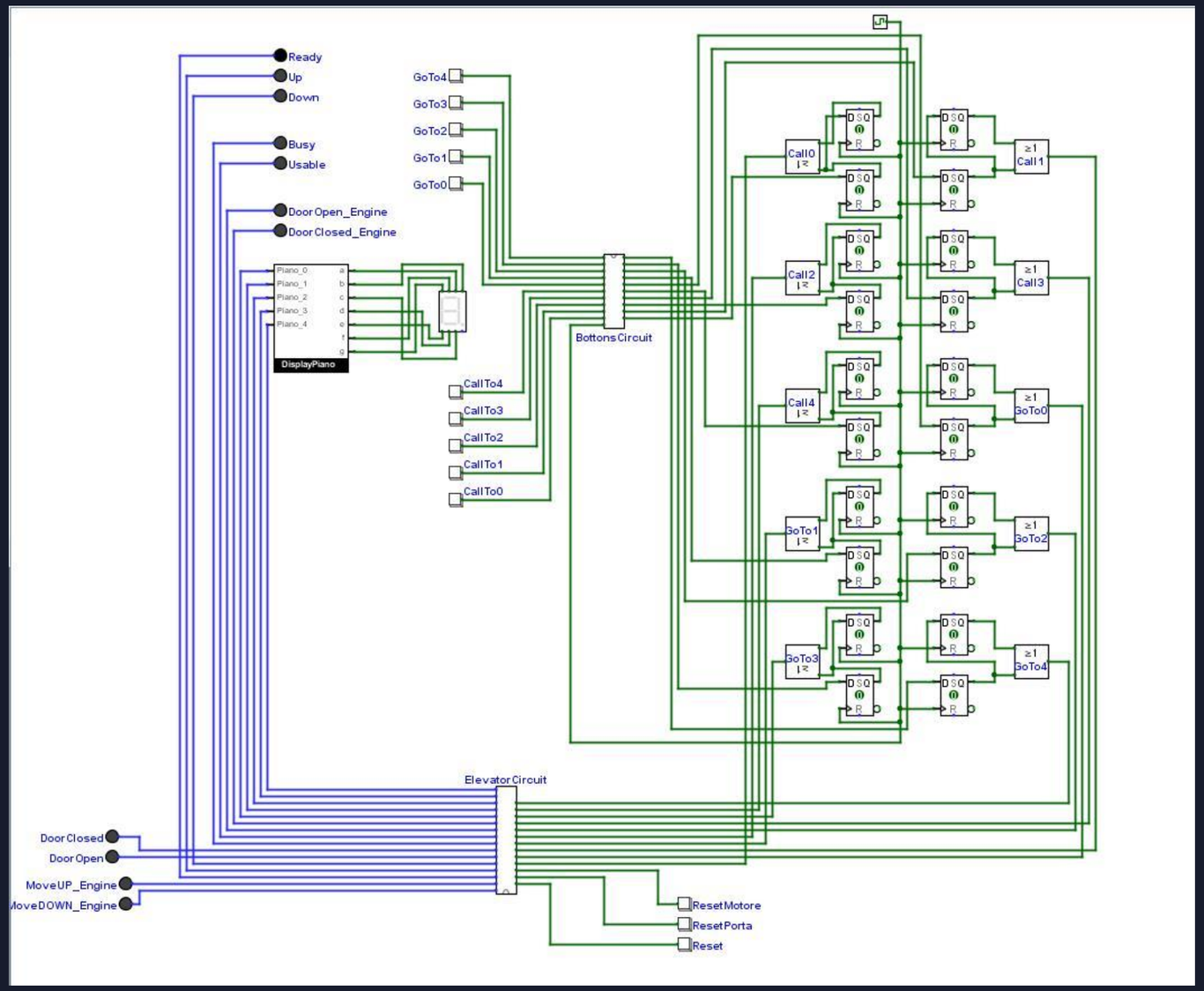
1997 2004 2009 2014 2019 2024

The Monster

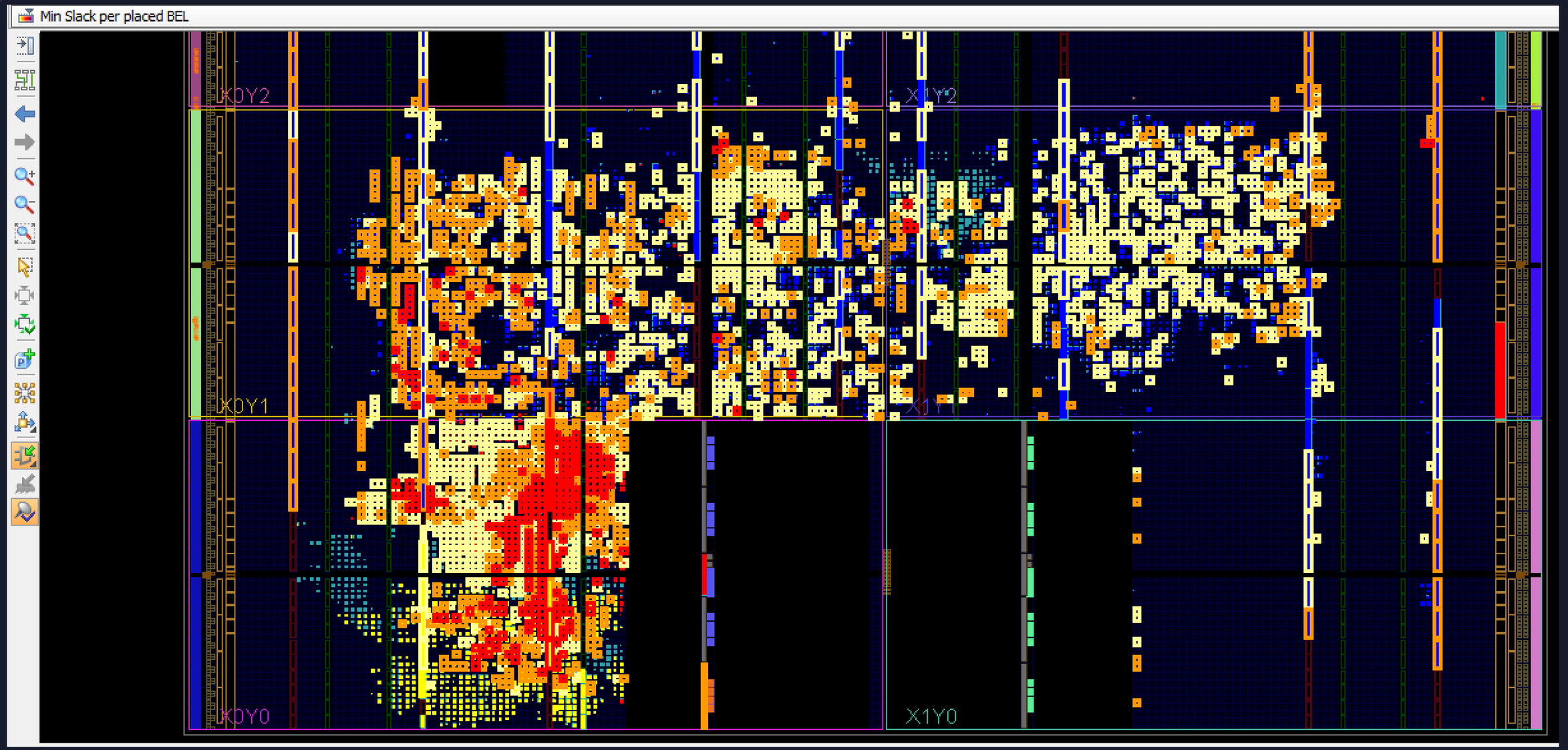
FPGAs

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity blinker_mod is
    Port(   clock1   :  in    STD_LOGIC;
            ALLOUT   :  out   STD_LOGIC_VECTOR (9 downto 0));
end blinker_mod;

architecture Behavioral of blinker_mod is
   SIGNAL   MainClk     : STD_LOGIC          := '0';          -- internal clock
   SIGNAL   MainCounter : UNSIGNED           (16 DOWNTO 0);   -- count range from 0 to 131071 (2^16)
   SIGNAL   RESET       : STD_LOGIC          := '0';          -- currently not used

   type state_type is (ST0,ST1,ST2,ST3,ST4,ST5,ST6,ST7,ST8,ST9);
   attribute ENUM_ENCODING: STRING;
   attribute ENUM_ENCODING OF state_type: type is "0100000011 0100100011 0101100011 0000000011 0010000011 0000010011 0100010
   SIGNAL STATE: state_type := ST0;                          -- my type definition

begin

   COUNT: PROCESS(RESET,MainClk)
   BEGIN
      IF    (RESET = '1' or MainCounter >= "11010110110110000") THEN MainCounter <= (OTHERS => '0');  -- 110000 clock cycles
      ELSIF (RISING_EDGE(MainClk)) THEN MainCounter <= MainCounter + 1;
      END IF;
   END PROCESS COUNT;


   SLOW: PROCESS(MainClk)
   BEGIN
      -- pause for 1us ~ 20clk cycles with MAINCLK @ 20MHz
      IF    (MainCounter = "00000000000010100") THEN STATE <= ST1;   -- @ 20 clk cycle    TG transfer gate open
      ELSIF (MainCounter = "00000000000010101") THEN STATE <= ST2;   -- @ 21 clk cycle    PG photo gate open
      ELSIF (MainCounter = "00000000000011110") THEN STATE <= ST1;   -- @ 30 clk cycle    PG photo gate closed
      ELSIF (MainCounter = "00000000000011111") THEN STATE <= ST3;   -- @ 31 clk cycle    TG tranfer gate closed
      ELSIF (MainCounter = "00000000000100000") THEN STATE <= ST4;   -- @ 32 clk cycle    AG antiblooming gate open
      ELSIF (MainCounter = "00000000000101111") THEN STATE <= ST3;   -- @ 47 clk cycle    AG antiblooming gate closed
      END IF;
   END PROCESS SLOW;

MainClk <= clock1;
with STATE select
     ALLOUT <="0100000011" WHEN ST0,
              "0100100011" WHEN ST1,
              "0101100011" WHEN ST2,
              "0000000011" WHEN ST3,
              "0010000011" WHEN ST4,
              "0000010011" WHEN ST5,
              "0100010011" WHEN ST6,
              "0100000010" WHEN ST7,
              "0100011101" WHEN ST8,
              "1100000011" WHEN ST9,
              "0100000011" WHEN OTHERS;
end Behavioral;
```

FPGAs


Ready
Up
Down
Busy
Usable
Door Open_Engine
Door Closed_Engine
GoTo4
GoTo3
GoTo2
GoTo1
GoTo0
Piano_0
Piano_1
Piano_2
Piano_3
Piano_4
DisplayPiano
CallTo4
CallTo3
CallTo2
CallTo1
CallTo0
Bottons Circuit
Call0
Call1
Call2
Call3
Call4
GoTo1
GoTo2
GoTo3
GoTo4
GoTo0
Elevator Circuit
Door Closed
Door Open
MoveUP_Engine
MoveDOWN_Engine
Reset Motore
Reset Porta
Reset

FPGAs



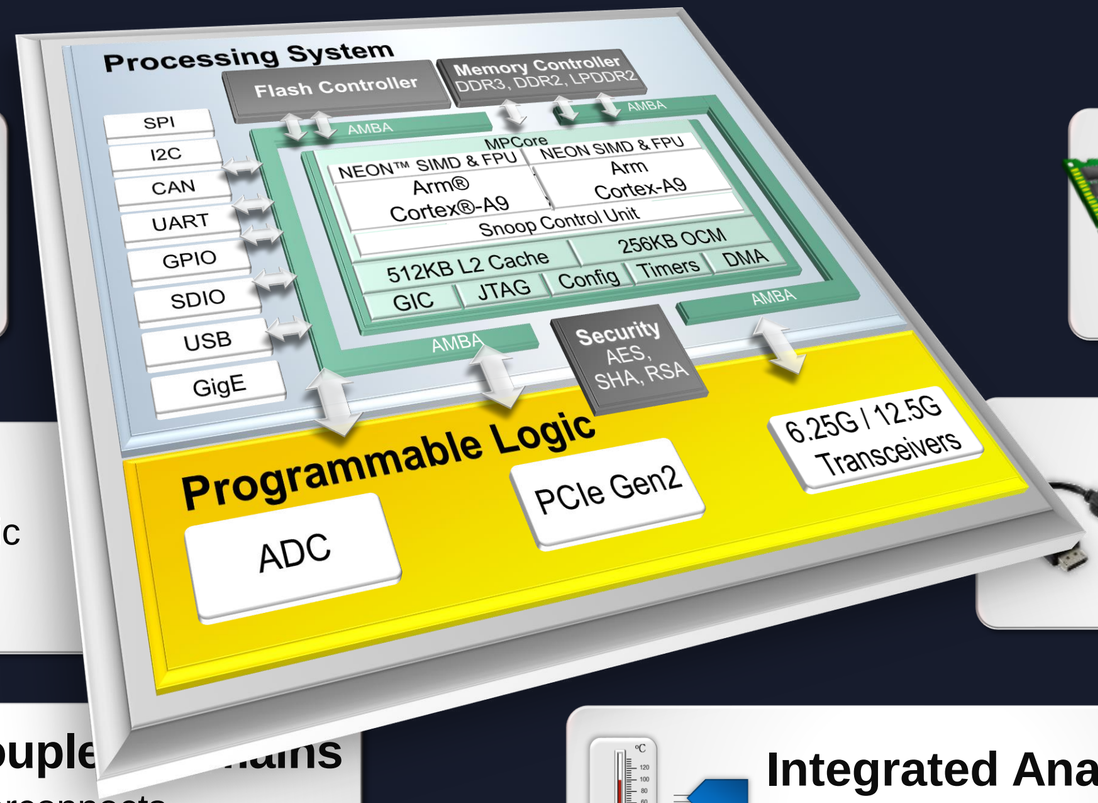
The Solution

SoC

Single-Core
766MHz
Artix-7 FPGA Fabric

Dual-Core
800MHz
Artix-7 FPGA Fabric

Dual Core
1GHz
Kintex-7 FPGA Fabric



Application Processor

- Single or Dual Core
- Up to 1GHz

High BW Memory

- L1/L2 Cache, OCM
- DDR2/3, LPDDR2 w/ECC

FPGA Fabric

- 7 Series FPGA Fabric
- Custom Engines

Integrated Peripherals

- USB, GigE, CAN
- UART, SDIO, I2C, SPI

Tightly Couple

- 3000+ interconnects
- Up to 100Gb/s Bandwidth

Integrated Analog

- Temp & Power Monitor
- 12-bit 1MSPS ADC

Mais periféricos?

Drag & Drop
100’s de IP & Peripherals

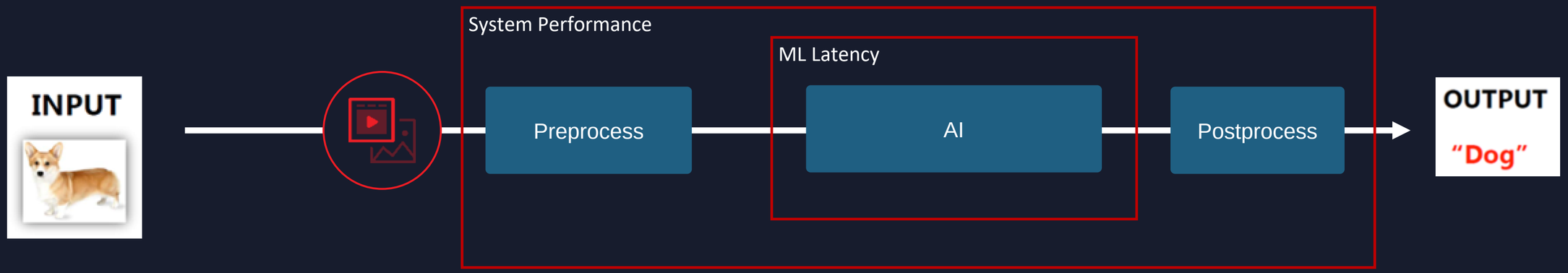
- IP Catalog
  - Partner IP
  - Automotive & Industrial
    - CAN
    - . . .
  - Embedded
  - Networking
  - Video & Image Processing
  - Digital Signal Processing

Drag, Drop, and Customize

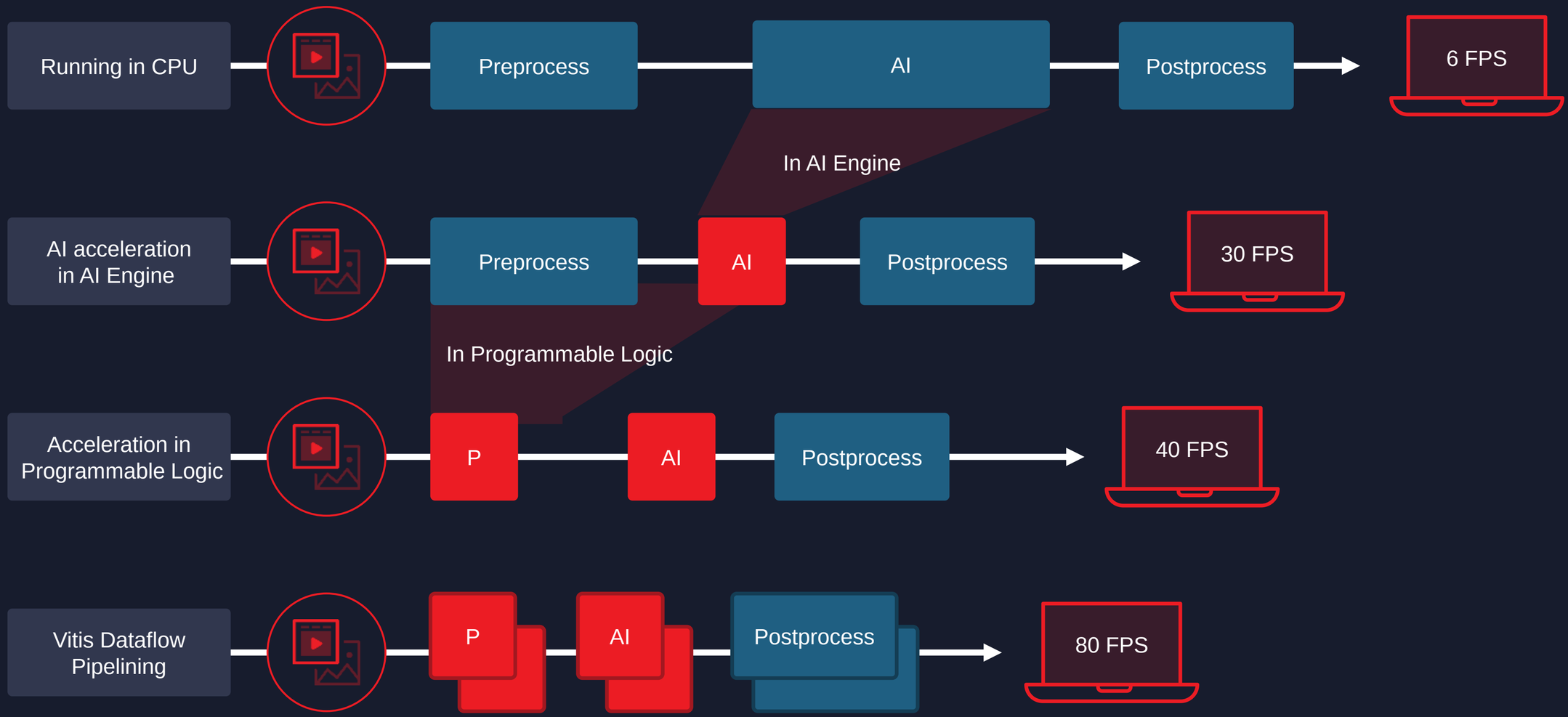
- ✓ **Expand Interfaces and Features**
- ✓ Adopt New Protocols *(e.g., EtherCAT, TSN, …)*
- ✓ Develop a “**Future-Proof**” project that evolves with market trends

Application Example: Smart Camera

Architecture for Smart Camera



Adaptive Architecture for Smart Camera



Vitis: Unified Software Platform

Coming soon…

Domain-specific development environment

Vitis accelerated libraries

Vitis core development kit

OpenCV Library

BLAS Library

Finance Library

TensorFlow

Vitis AI

FFmpeg

Vitis Video

Partners
Genomics, Data Analytics, And more

Compilers

Analyzers

Debuggers

Xilinx runtime libraries (XRT)

Vitis target platform

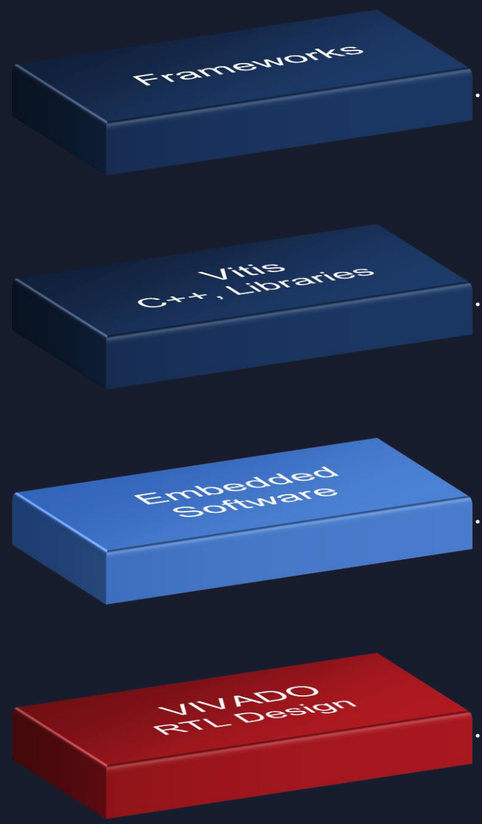
Putting it All Together

AI Scientists
(iterations in minutes)

Application
Software Developers

Embedded
Developers

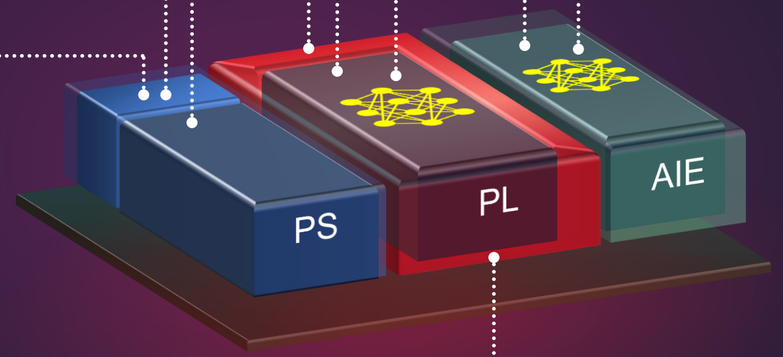
Hardware
Developers



TensorFlow

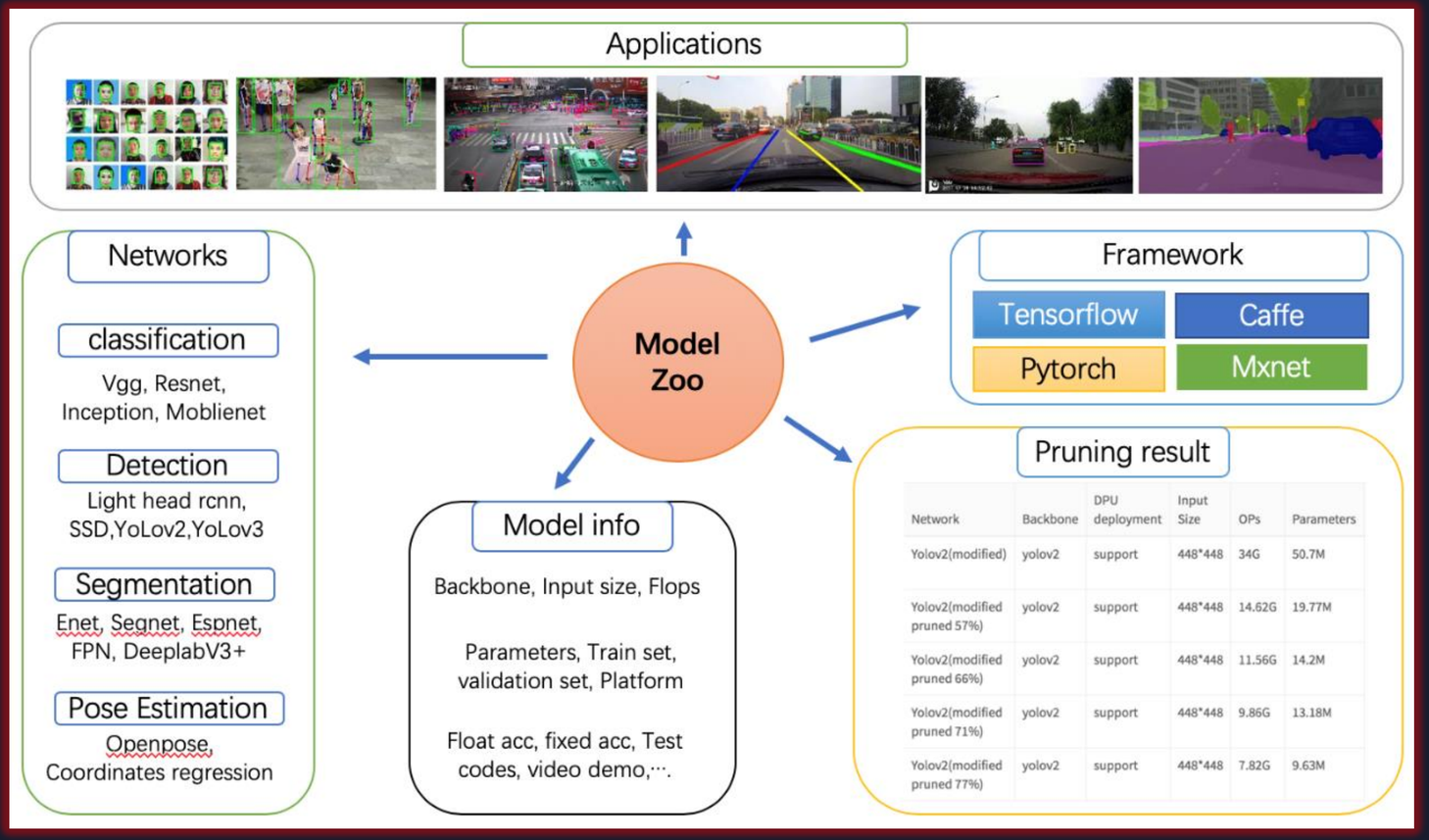
python

OpenCV



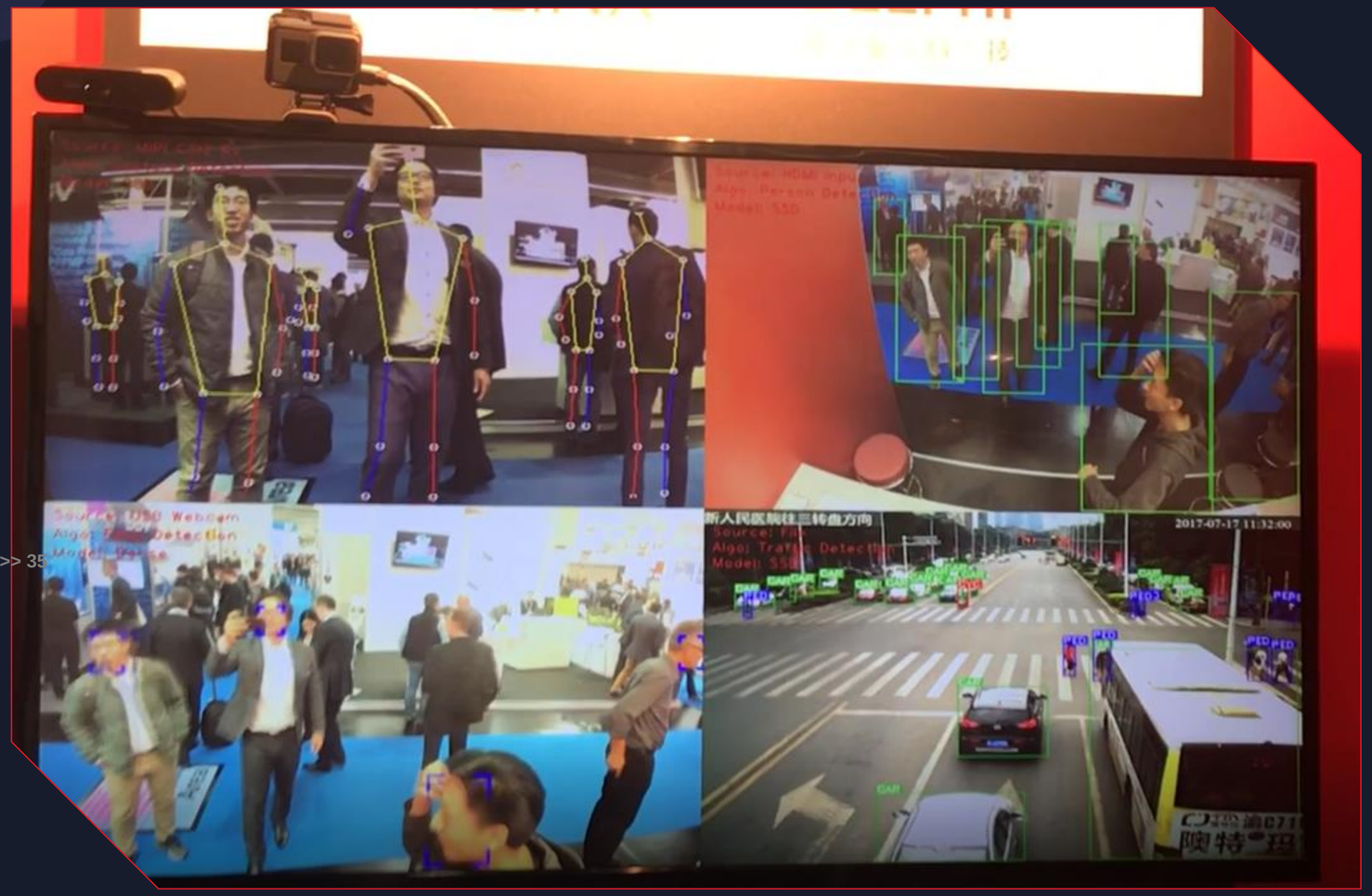
VITIS AI Model Zoo

- ✓ **Open for all users**
- ✓ **Leveraging mainstream frameworks and networks**
- ✓ **Deployable and re-trainable**



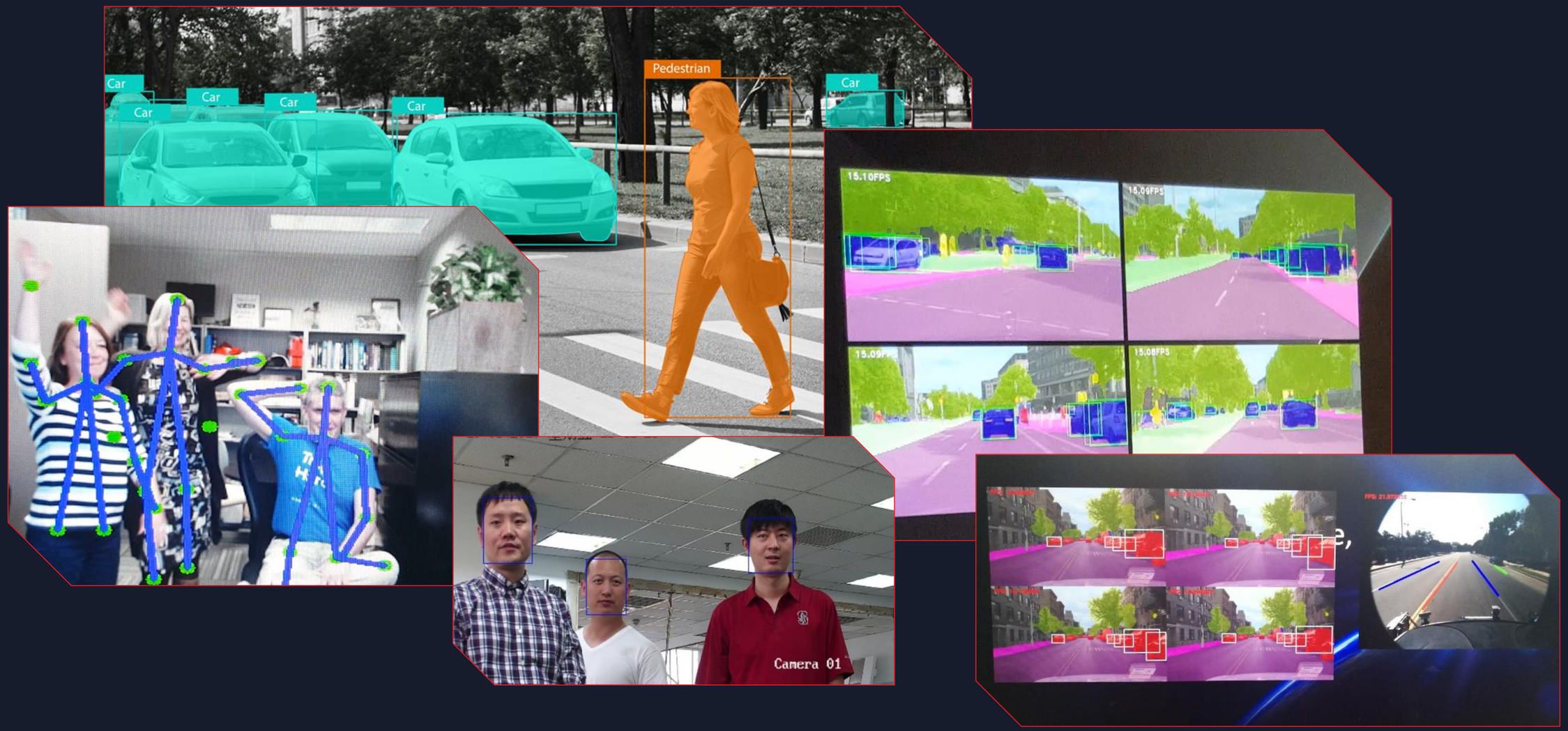
Application	Module
Face	Face detection
	Landmark Localization
	Face recognition
	Face attributes recognition
Pedestrian	Pedestrian Detection
	Pose Estimation
	Person Re-identification
Video Analytics	Object detection
	Pedestrian Attributes Recognition
	Car Attributes Recognition
	Car Logo Detection
	Car Logo Recognition
	License Plate Detection
	License Plate Recognition
ADAS/AD	Object Detection
	3D Car Detection
	Lane Detection
	Traffic Sign Detection
	Semantic Segmentation
	Drivable Space Detection

Single-chip Deployment of Multiple Models



- ✓ Multi-task
- ✓ Multi-model
- ✓ Multi-framework
- ✓ Cascaded inference
- ✓ One or more DPU instances
- ✓ Custom layer types
- ✓ Graph segmentation
- ✓ One bitstream supports many CNNs

Edge Deployment of Custom Models

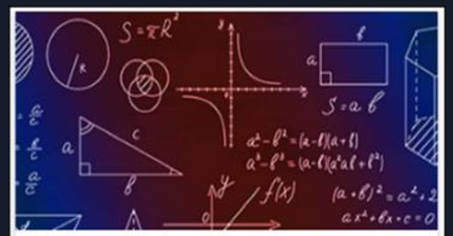


Extensive Open Source Libraries

400+ functions across 8 libraries
Open source, performance-optimized out-of-the-box acceleration

GitHub

- Library
  - Docs
    - Source
    - Tests
    - Examples
    - Benchmarks


Vitis BLAS Library **25 functions**


Vitis Solver Library **12**


Vitis Security Library **99**


Vitis Vision Library **114**


Vitis Data Compression Library **25**

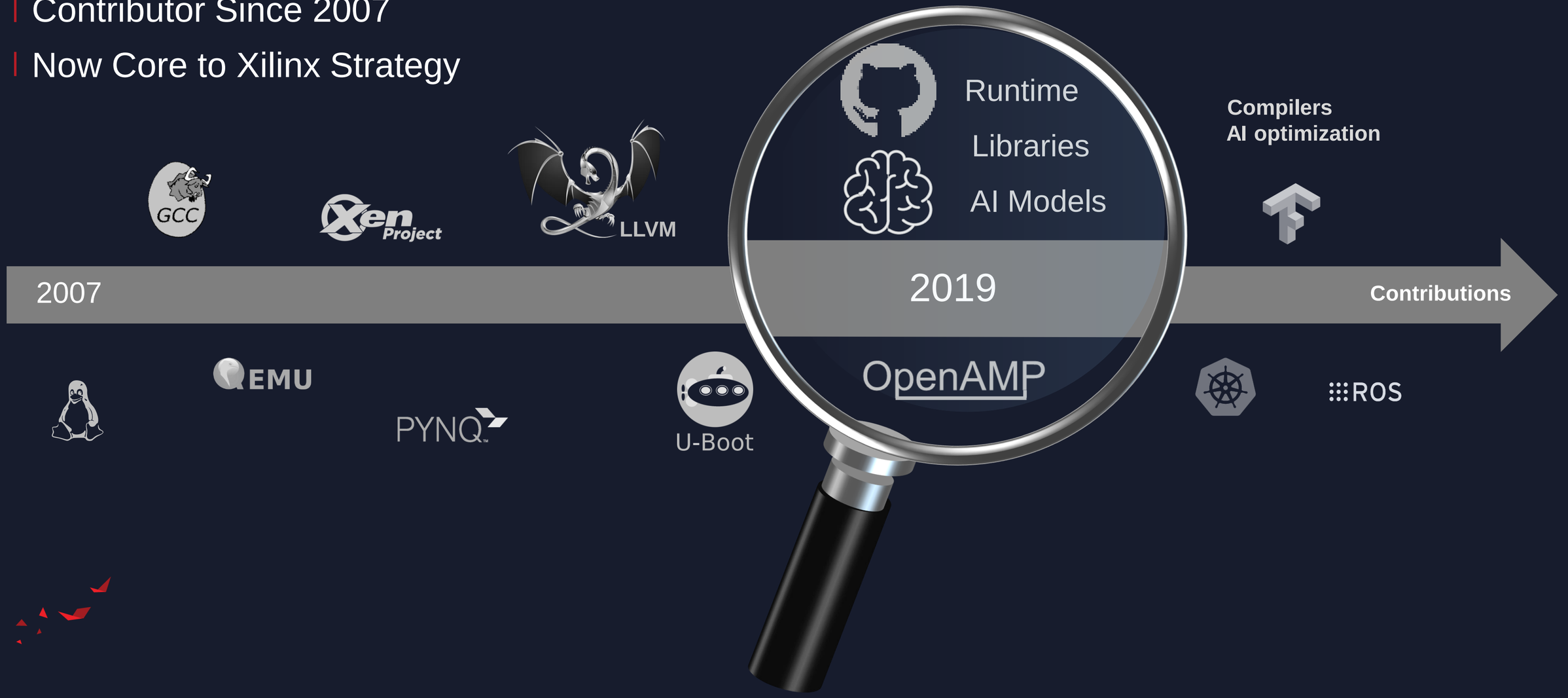

Vitis Quantitative Finance Library **55**


Vitis Database Library **36**

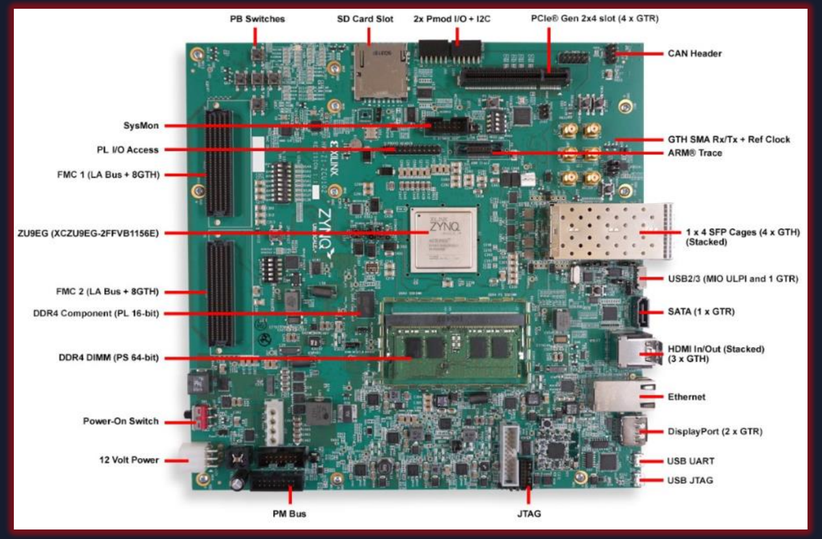

Vitis AI Library **37 Models**

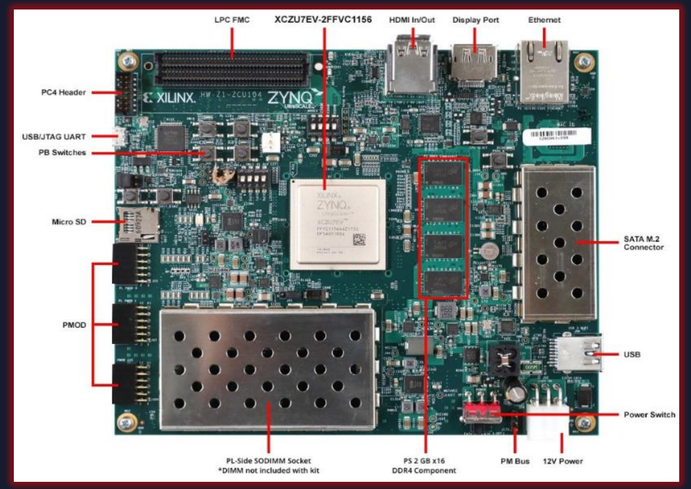
Committed to Open Source

- User Since 2001
- Contributor Since 2007
- Now Core to Xilinx Strategy



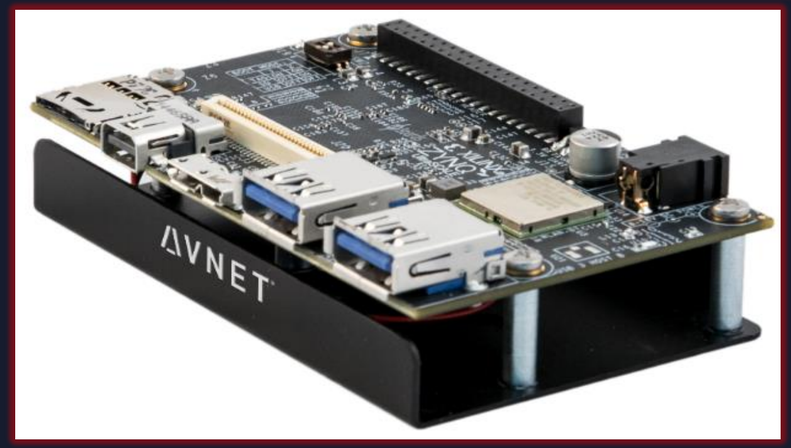
AI Developer Hub

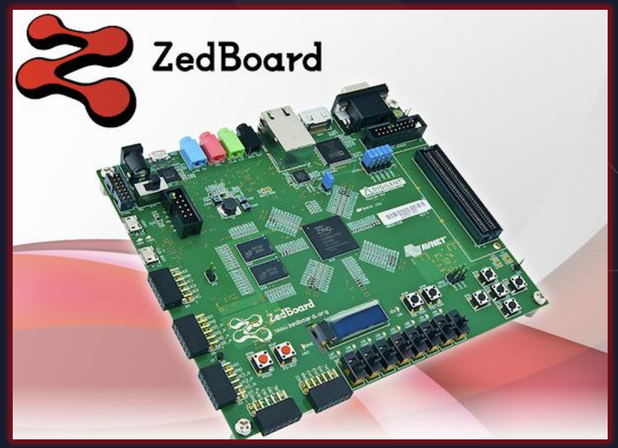




Edge AI Evaluation Boards

Product	Documentation	Image Download	DNNDK Version	File Size	MD5 Checksum
ZCU102 Kit	ZCU102 User Guide (UG1182)	petalinux-user-image-zcu102-zynqmp-sd-20190802.img.gz	V3.1	311 MB	1d67b1380ffef0da18d923deb92b5f6b
		xilinx-zcu102-prod-dpu1.4-2018.3-desktop-buster-2019-04-24.img.zip	v3.0	657 MB	d49eab4d293d8d1af40fcc369e1c4f53
		2018-12-04-zcu102-desktop-stretch.img.zip	v2.08	571 MB	d0d5faf8ece80b96f5591d09756d5a5d
ZCU104 Kit	ZCU104 User Guide (UG1267)	petalinux-user-image-zcu104-zynqmp-sd-20190802.img.gz	V3.1	311 MB	a238b286651fbb308cec923664980b34
		xilinx-zcu104-prod-dpu1.4-desktop-buster-2019-04-23.img.zip	v3.0	655 MB	503661dd1ee4549a562775034b95d0c8
		2018-12-04-zcu104-desktop-stretch.img.zip	v2.08	571 MB	ada2420c4afbd89efdeea741e0917e26
Avnet Ultra 96	Ultra 96 User Guide	petalinux-user-image-ultra96-zynqmp-sd-20190802.img.gz	v3.1	537 MB	aee8464d0fd52776567f28a221c80c71
		xilinx-ultra96-prod-dpu1.4-desktop-buster-2019-05-31.img.zip	v3.0	576 MB	c9c6a5f5a772077abc8fffde6ea8f3db
		xilinx-ultra96-desktop-stretch-2018-12-10.img.zip	v2.08	566 MB	c5d2422063213b4bc4c18a3223c6adc8
Avnet Zedboard	Zedboard User Guide	xilinx-zedboard-dnndk3.1-image-20190812.zip	v3.1	315 MB	36706f19ec949ad964f6ab328f874e88

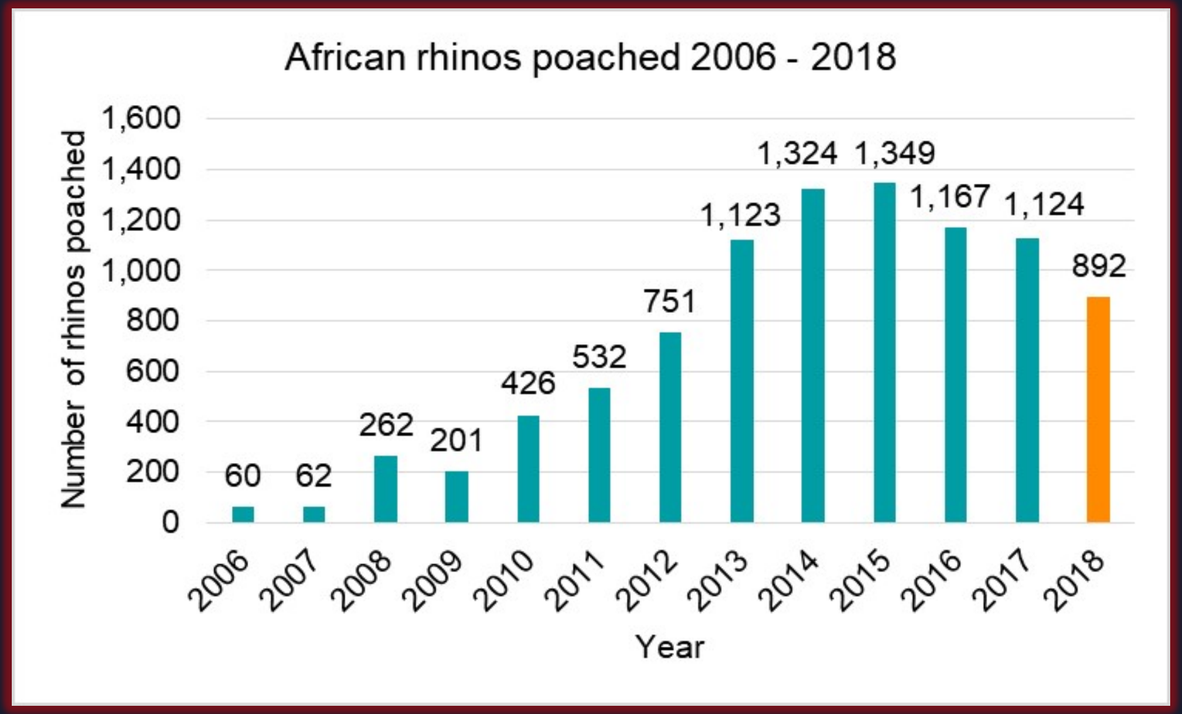




XILINX.

What about Rhinos?

In the last decade 8,889 African Rhinos have been lost to poaching

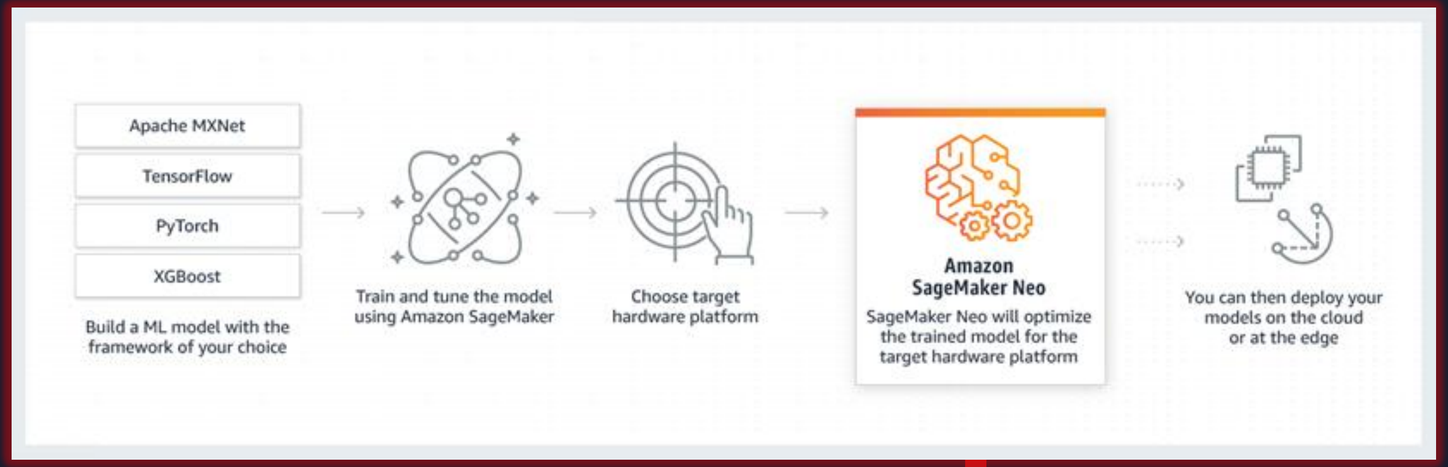


Source: https://www.savetherhino.org/rhino-info/poaching-stats/

More than 900 Rhinos are still being poached each year

XILINX.

Kutleng Engineering Technologies - SmartCAM



aws

Kutleng ENGINEERING TECHNOLOGIES

CNN DPU

AWS IoT Greengrass

XILINX

FPGAs - Brave New World

MATLAB® & SIMULINK®

PYNQ™

yocto PROJECT

VHDL
Very High Speed Integrated Circuit Hardware Description Language

VERILOG

Caffe

Building the Adaptable, Intelligent World